IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

GEOTAG IP, LLC,	)	
Plaintiff	)	
	)	
	)	**Civil Action 6:22-cv-00125**
v.	)	
	)	
NXP USA, INC.,	)	
Defendant.	)	**JURY TRIAL DEMANDED**
	)	

PLAINTIFF'S ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Geotag IP, LLC ("Geotag") files this Original Complaint and demand for jury trial seeking relief from patent infringement of the claims of U.S. Patent No. 9,511,910 ("the '910 patent") (referred to as the "Patent-in-Suit") by NXP USA, Inc., ("NXP").

I. THE PARTIES

1. Plaintiff Geotag is a Texas Limited Liability Company with its principal place of business located in Travis County, Texas.

2. On information and belief, NXP is a corporation existing under the laws of Delaware, with a principal place of business located at 6501 William Cannon Drive West, Austin, TX 78735. On information and belief, NXP sells and offers to sell products and services throughout Texas, including in this judicial district, and introduces products and services that perform infringing methods or processes into the stream of commerce knowing that they would be sold in Texas and this judicial

district. NXP may be served through their registered agent Corporation Service Company dba CSC – Lawyers incorporating Service Company, 211 E. 7th St, Suite 620, Austin, TX 78701-3218.

II. JURISDICTION AND VENUE

3. This Court has original subject-matter jurisdiction over the entire action pursuant to 28 U.S.C. §§ 1331 and 1338(a) because Plaintiff's claim arises under an Act of Congress relating to patents, namely, 35 U.S.C. § 271, et. seq.

4. This Court has personal jurisdiction over Defendant because: (i) Defendant is present within or has minimum contacts within the State of Texas and this judicial district; (ii) Defendant has purposefully availed itself of the privileges of conducting business in the State of Texas and in this judicial district; and (iii) Plaintiff's cause of action arises directly from Defendant's business contacts and other activities in the State of Texas and in this judicial district.

5. Venue is proper in this district under 28 U.S.C. §§ 1391(b) and 1400(b). Defendant has committed acts of infringement and has a regular and established place of business in this District. Further, venue is proper because Defendant conducts substantial business in this forum, directly or through intermediaries, including: (i) at least a portion of the infringements alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent courses of conduct and/or deriving substantial revenue from goods and services provided to individuals in Texas and this District.

III. INFRINGEMENT

A. Infringement of the '910 Patent

6. On December 6, 2016, U.S. Patent No. 9,511,910 ("the '910 patent", attached as Exhibit A) entitled "Intelligent Wine Capsule" was duly and legally issued by the U.S. Patent and Trademark Office. Geotag owns the '910 patent by assignment.

7. The '910 patent relates to a datalogger that includes energy harvesting and use.

8. NXP makes, uses, and sells dataloggers including energy harvesting, in particular their integrated circuits optimized for monitoring and logging, and use that infringes one or more claims of the '910 patent, including independent claim 20, literally or under the doctrine of equivalents. Defendant put the inventions claimed by the '910 Patent into service (i.e., used them); but for Defendant's actions, the claimed-inventions embodiments involving Defendant's products and services would never have been put into service. Defendant's acts complained of herein caused those claimed-invention embodiments as a whole to perform, and Defendant's procurement of monetary and commercial benefit from it.

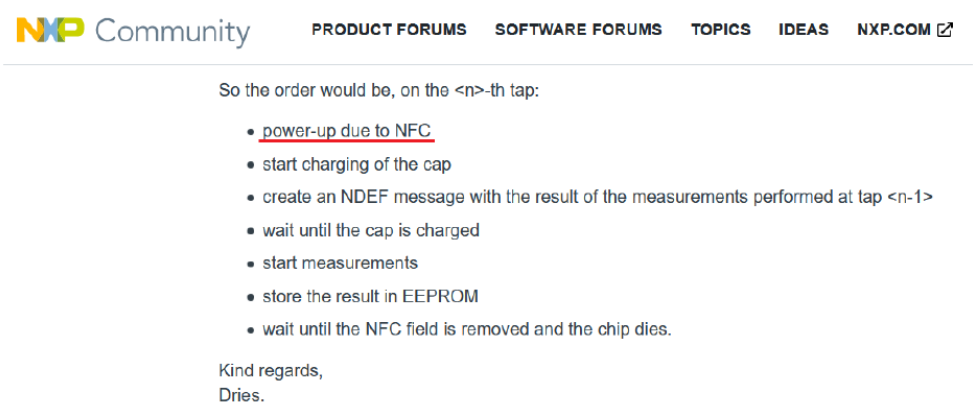
9. Support for the allegations of infringement may be found in the following preliminary table:

US 9511910 B2 Claim 20	NXP's Wireless Energy Harvesting Sensor Node
20. A method comprising: receiving electromagnetic energy at an energy harvester to form harvested electromagnetic energy;	As per the NXP NHS31xx user manual, NHS31xx performs a method comprising, receiving electromagnetic energy (i.e., energy received via Smartphone NFC) at an energy harvester (i.e., NFC rectifier) to form harvested electromagnetic energy (i.e., rectified NFC power). The NHS31xx brochure and and company representative statements in the company's community forum indicates the NHX31xx can be powered by harvesting energy from NFC. NHS31xx contains an NFC rectifier (i.e., harvester) and capacitors to store the NFC power. **1.1 Introduction** The NHS31xx are a family of ICs optimized for monitoring and logging. With their embedded NFC interface, internal temperature sensor and direct battery connection, they support effective system solutions with a minimal number of external components. The embedded ARM Cortex-M0+ offers flexibility to the users of these ICs to implement their own dedicated solution. The NHS31xx family contains multiple features, like a selectable CPU frequency of up to 8 MHz and various power-down modes for ultra-low-power consumption. Users can program this NHS31xx family with the industry-wide standard solutions for ARM Cortex-M0+ processors. Peripheral components include an ultra-low-power RTC, I^2C-bus interface, SPI interface with SSP features, NFC wireless interface and up to 12 general-purpose I/O pins. Depending on the chip variant, other features include a temperature sensor, specific interfaces for capacitive, resistive and current measurements, and a 12-bit ADC/DAC. There are also specific analog interfaces for interfacing with photodiodes and LEDs. Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 3) **5.4 System power architecture** The NHS31xx platform accepts power from two different sources: from the external power supply pin VDDBAT (domain VBAT), or from the built-in NFC/RFID rectifier (domain VNFC). VDD_ALON via the VDD_ALON pad powers the external ring (VDDE) of the IO pads, as shown in Figure 8. ***Note:*** *the pad ring does not power the VDDBAT pin, it is thus not possible to power external devices connected to this pin. In Passive RF mode, external devices can be powered by connecting them to a PIO0_n (preferably a high-drive pin) set to output logic 1.* The PMU in the always-on domain then decides on the powering of the internal domains. The power source decision is as follows: • If voltage is detected on VBAT and not on VNFC, VBAT powers the internal domains • If voltage < 1.72 V is detected on VBAT, and higher voltage is detected on VNFC, VNFC powers the internal domains • If voltage > 1.72 V is detected at both VBAT and VNFC, VBAT powers the internal domains Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 35)

Optimized for event logging	Multiple event detection mechanisms (resistive capacitive or GPIO) Event control (pin-change or wake-up)
Flexible	Customer-programmable ARM Cortex M0+ processor industry class ARM development tools
Low power	Battery start enabling via NFC (extends shelf life) Over-the-air powered (NFC)
Highly integrated	Embedded non-volatile data logging storage (up to 32KB) No crystal
Interfaces	NFC for readout and parameter writing and power GPIO pins for visual feedback (e.g. LED) SPI and I²C

Source: https://www.nxp.com/docs/en/brochure/75017700.pdf (Page: 3)

Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true



Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true

	The VNFC input power net contains a buffer capacitor to maintain system integrity during Miller pauses when powered from RF field. Each pause lasts 3 µs, and the voltage drop should be limited to 0.4 V (1.4 V at input of 1.2 V LDO). The average current is assumed at 150 µA. In this case, the minimum size for the buffer capacitor is: $C = \frac{\Delta Q}{\Delta V} = \frac{150\ \mu A \times 3\ \mu s}{0.4\ V} = 1.125\ nF$ (1) For passive RFID powered operation, adding an external 100 nF capacitor on PIO0_x pins set to logic 1 is recommended. Adding this capacitor ensures that all operations are possible during Miller pauses (e.g. Flash write). Source: http://www.farnell.com/datasheets/2337743.pdf (Page: 36) • The user can force the selection of the VBAT input by disabling the automatic power switch, which disables the automatic source selector voltage comparator. When on NFC power only (passive operation), connect one or more 100 nF external capacitors in parallel to a GPIO pad and set that pad as an output driven to logic 1. A high-drive pin should preferably be chosen and several pins can be connected in parallel. PSWNFC and PSWBAT are the power switches. PSWNFC connects power to the VDD_ALON power net when an RF field is present. PSWBAT connects power from the Source: https://www.nxp.com/docs/en/data-sheet/NHS3100.pdf (Page: 36)

transferring the harvested electromagnetic energy to at least one energy storage component to form stored energy;	As per the NXP NHS31xx user manual and company representative statements in the company's community forum, NHS31xx can be configured to perform a method comprising, transferring the harvested electromagnetic energy (i.e., rectified NFC power) to at least one energy storage component (i.e., capacitors) to form stored energy (i.e., energy stored in the capacitors which can support all operations of the chip).

5.4 System power architecture

The NHS31xx platform accepts power from two different sources: from the external power supply pin VDDBAT (domain VBAT), or from the built-in NFC/RFID rectifier (domain VNFC).

VDD_ALON via the VDD_ALON pad powers the external ring (VDDE) of the IO pads, as shown in Figure 8.

Note: *the pad ring does not power the VDDBAT pin, it is thus not possible to power external devices connected to this pin. In Passive RF mode, external devices can be powered by connecting them to a PIO0_n (preferably a high-drive pin) set to output logic 1.*

The PMU in the always-on domain then decides on the powering of the internal domains.

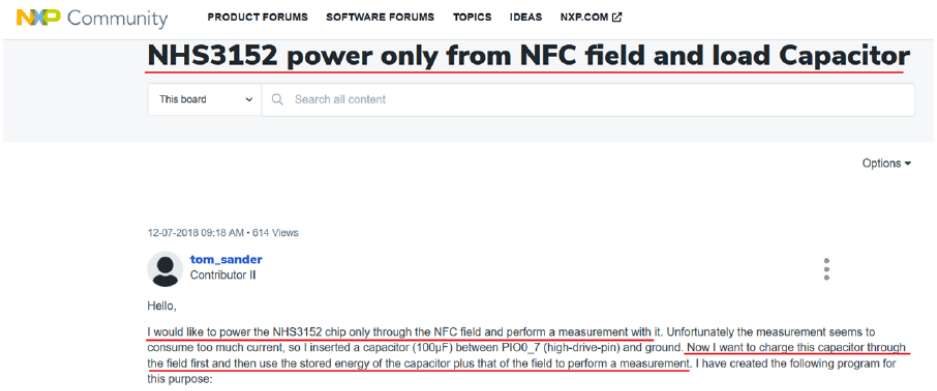
The power source decision is as follows:

- If voltage is detected on VBAT and not on VNFC, VBAT powers the internal domains
- If voltage < 1.72 V is detected on VBAT, and higher voltage is detected on VNFC, VNFC powers the internal domains
- If voltage > 1.72 V is detected at both VBAT and VNFC, VBAT powers the internal domains

Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 35)

18:17	FORCEVBAT FORCEVNFC	-	force the power source selection	0
		01	force to VBAT/external power	
		10	force to NFC power	
		11	autoswitching if PMULPM is 0	

Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 41)



Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true

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So the order would be, on the <n>-th tap:

- power-up due to NFC
- start charging of the cap
- create an NDEF message with the result of the measurements performed at tap <n-1>
- wait until the cap is charged
- start measurements
- store the result in EEPROM
- wait until the NFC field is removed and the chip dies.

Kind regards,
Dries.

Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true

The VNFC input power net contains a buffer capacitor to maintain system integrity during Miller pauses when powered from RF field. Each pause lasts 3 µs, and the voltage drop should be limited to 0.4 V (1.4 V at input of 1.2 V LDO). The average current is assumed at 150 µA. In this case, the minimum size for the buffer capacitor is:

$$C = \frac{\Delta Q}{\Delta V} = \frac{150\ \mu A \times 3\ \mu s}{0.4\ V} = 1.125\ nF \quad (1)$$

For passive RFID powered operation, adding an external 100 nF capacitor on PIO0_x pins set to logic 1 is recommended. Adding this capacitor ensures that all operations are possible during Miller pauses (e.g. Flash write).

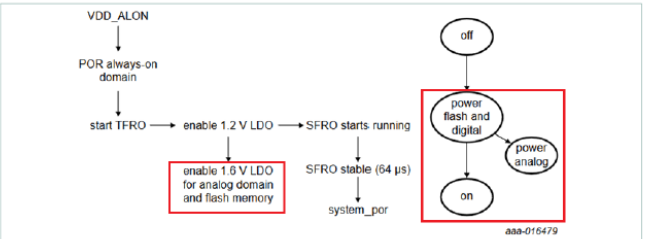
Source: http://www.farnell.com/datasheets/2337743.pdf (Page: 36)

- The user can force the selection of the VBAT input by disabling the automatic power switch, which disables the automatic source selector voltage comparator.

When on NFC power only (passive operation), connect one or more 100 nF external capacitors in parallel to a GPIO pad and set that pad as an output driven to logic 1. A high-drive pin should preferably be chosen and several pins can be connected in parallel.

PSWNFC and PSWBAT are the power switches. PSWNFC connects power to the VDD_ALON power net when an RF field is present. PSWBAT connects power from the

Source: https://www.nxp.com/docs/en/data-sheet/NHS3100.pdf (Page: 36)

	• Switchover between sources is possible. For example, if initially both VBAT and VNFC are available, the system is powered from VBAT. If VBAT then becomes unavailable because it is switched off externally or the PSWBAT power switch is overridden, the internal domains are immediately powered from VNFC. Switchover is supported in both directions • When on NFC power only (passive operation), a PROGRAM or ERASE operation on the FLASH memory will cause a severe voltage drop, causing a reset. To enable the possibility to PROGRAM, capacitors must be added externally. – The use of 2 capacitors is preferred to lower the serial resistance. – Connect each 220 nF capacitor to a GPIO pin, with the other side of the capacitor tied to ground. – PIO3, PIO7, PIO10 and PIO11 have the lowest resistive values when the ultra-high drive mode - see Table 252 - is enabled. The use of these pins is therefor preferred. In firmware, these capacitors must be put to use according to this sequence, before a PROGRAM operation is started: 1. Configure both pins as input with pull-up enabled. This will ensure a slow build-up of the charge in the capacitor. 2. Wait until the capacitors are almost fully charged. The exact time to wait can be calculated in advance. In addition, the pin value can be continually read until it reads a 1. This provides the earliest time possible to move to the next step. 3. Reconfigure the pins as output. When changing the direction, the value that is output on the pin is not taken from the corresponding register. Instead, it is sampled from what was provided when the pin was still an input. If the capacitor is not sufficiently charged, it will output a 0. If enough time was spent waiting in the second step above, the value will become a 1. The reconfiguration is necessary to provide a low resistance path between the capacitor and the internal voltage rail. This ensures the charge can be used to overcome the current peak that occurs while flashing. Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 36) The power-up sequence is shown in Figure 11. When external power is applied and the PSUBAT switch closed, the always-on part gets a power-on reset signal and the timer FRO starts running. The TFRO starts a small state machine in the PMU. In the first state, the LDO powering the digital domain is started. In the second state, the LDO powering the 1.6 V analog domain is started. In the last state, the system is considered 'on'. The transition from 'off' to 'on' takes approximately 92 µs. In the VDD1V2 domain, enabling the LDO1 and SFRO triggers the system_por. The system can boot when the Flash memory is operational. If there is no external power, but there is RF power, the same procedure is followed except that PSWNFC connects power to the LDOs.  Figure 11. NHS31xx power-up sequence Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 39)

after a voltage of the stored energy exceeds a pre-defined threshold, turning ON at least one	As per the NXP NHS31xx user manual and company representative statements in the company's community forum, the NXP NHS31xx is configured to perform a method comprising, wherein, after a voltage of the stored energy (i.e., VNFC, power stored in capacitors) exceeds a pre-defined threshold (i.e., 1.72V), turning ON (i.e., the system is considered on) at least one processor (i.e., ARM M0+ core) and at least one non-volatile memory (i.e., non-volatile memory like EEPROM) wherein the at least one processor (i.e., ARM M0+ core) and the at least one non-volatile memory

processor and at least one non-volatile memory, wherein the at least one processor and the at least one non-volatile memory are powered by the stored energy;	(i.e., non-volatile memory like EEPROM) are powered by the stored energy (i.e. harvest NFC power stored in a capacitor). The NHS31XX documentation indicates the internal domain is completely powered by the VNFC after it exceeds a voltage of 1.72V when only NFC is available. Further, NHS31xx can be configured to perform temperature measurements and stores them in EEPROM, after the capacitor is charged. **5.3.1 Active mode** Active mode is the only mode in which the ARM core is executing instructions. The system clock, or a dedicated peripheral clock, clocks the peripherals. The chip is in Active mode after reset. The reset values of the PDRUNCFG and SYSAHBCLKCTRL registers determine the default power configuration (see Section 4.5.6). The power configuration can be changed during runtime. Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 32) 18:17 FORCEVBAT FORCEVNFC - force the power source selection 0 01 force to VBAT/external power 10 force to NFC power 11 autoswitching if PMULPM is 0 Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 41) **5.4 System power architecture** The NHS31xx platform accepts power from two different sources: from the external power supply pin VDDBAT (domain VBAT), or from the built-in NFC/RFID rectifier (domain VNFC). VDD_ALON via the VDD_ALON pad powers the external ring (VDDE) of the IO pads, as shown in Figure 8. ***Note:*** *the pad ring does not power the VDDBAT pin, it is thus not possible to power external devices connected to this pin. In Passive RF mode, external devices can be powered by connecting them to a PIO0_n (preferably a high-drive pin) set to output logic 1.* The PMU in the always-on domain then decides on the powering of the internal domains. The power source decision is as follows: • If voltage is detected on VBAT and not on VNFC, VBAT powers the internal domains • If voltage < 1.72 V is detected on VBAT, and higher voltage is detected on VNFC, VNFC powers the internal domains • If voltage > 1.72 V is detected at both VBAT and VNFC, VBAT powers the internal domains Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 35)

The power-up sequence is shown in Figure 11. When external power is applied and the PSUBAT switch closed, the always-on part gets a power-on reset signal and the timer FRO starts running. The TFRO starts a small state machine in the PMU. In the first state, the LDO powering the digital domain is started. In the second state, the LDO powering the 1.6 V analog domain is started. In the last state, the system is considered 'on'. The transition from 'off' to 'on' takes approximately 92 µs. In the VDD1V2 domain, enabling the LDO1 and SFRO triggers the system_por. The system can boot when the Flash memory is operational.

If there is no external power, but there is RF power, the same procedure is followed except that PSWNFC connects power to the LDOs.

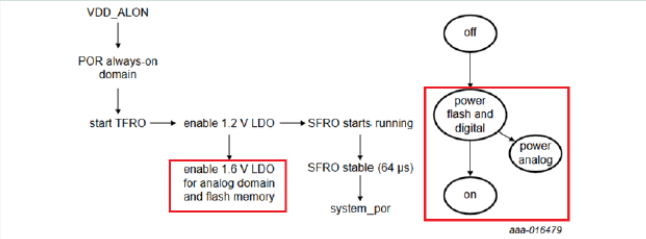
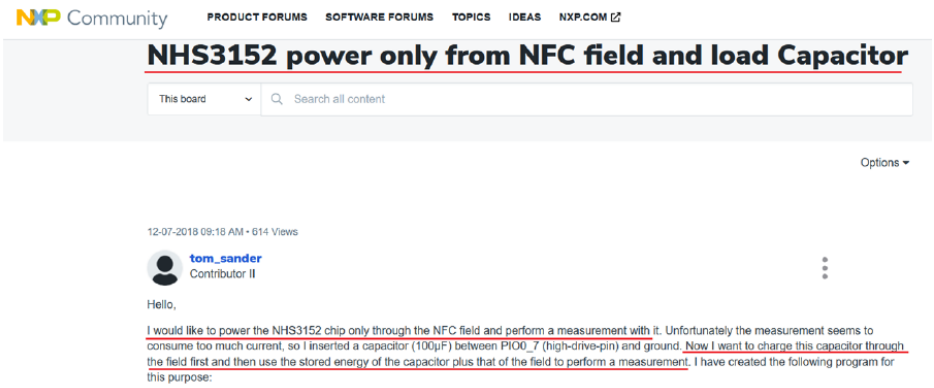
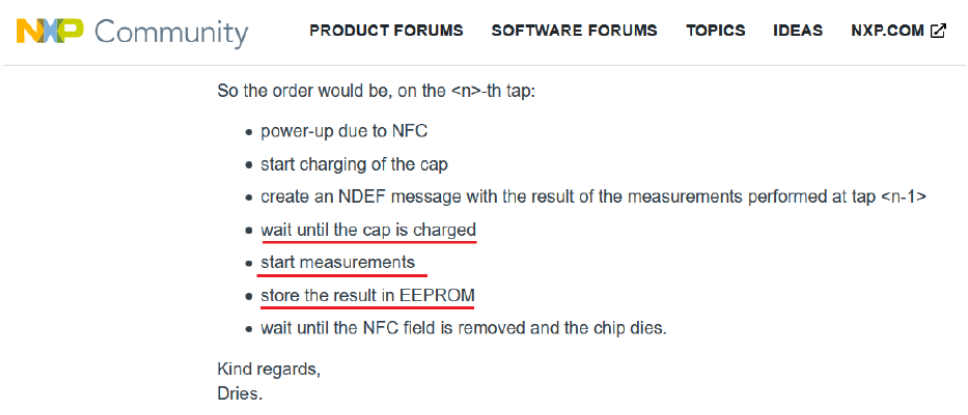


Figure 11. NHS31xx power-up sequence

Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 39)



Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true



Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true

	The VNFC input power net contains a buffer capacitor to maintain system integrity during Miller pauses when powered from RF field. Each pause lasts 3 µs, and the voltage drop should be limited to 0.4 V (1.4 V at input of 1.2 V LDO). The average current is assumed at 150 µA. In this case, the minimum size for the buffer capacitor is: $C = \frac{\Delta Q}{\Delta V} = \frac{150\ \mu A \times 3\ \mu s}{0.4\ V} = 1.125\ nF$ (1) For passive RFID powered operation, adding an external 100 nF capacitor on PIO0_x pins set to logic 1 is recommended. Adding this capacitor ensures that all operations are possible during Miller pauses (e.g. Flash write). Source: http://www.farnell.com/datasheets/2337743.pdf (Page: 36) • The user can force the selection of the VBAT input by disabling the automatic power switch, which disables the automatic source selector voltage comparator. When on NFC power only (passive operation), connect one or more 100 nF external capacitors in parallel to a GPIO pad and set that pad as an output driven to logic 1. A high-drive pin should preferably be chosen and several pins can be connected in parallel. PSWNFC and PSWBAT are the power switches. PSWNFC connects power to the VDD_ALON power net when an RF field is present. PSWBAT connects power from the Source: https://www.nxp.com/docs/en/data-sheet/NHS3100.pdf (Page: 36) • Switchover between sources is possible. For example, if initially both VBAT and VNFC are available, the system is powered from VBAT. If VBAT then becomes unavailable because it is switched off externally or the PSWBAT power switch is overridden, the internal domains are immediately powered from VNFC. Switchover is supported in both directions • When on NFC power only (passive operation), a PROGRAM or ERASE operation on the FLASH memory will cause a severe voltage drop, causing a reset. To enable the possibility to PROGRAM, capacitors must be added externally. – The use of 2 capacitors is preferred to lower the serial resistance. – Connect each 220 nF capacitor to a GPIO pin, with the other side of the capacitor tied to ground. – PIO3, PIO7, PIO10 and PIO11 have the lowest resistive values when the ultra-high drive mode - see Table 252 - is enabled. The use of these pins is therefor preferred. In firmware, these capacitors must be put to use according to this sequence, before a PROGRAM operation is started: 1. Configure both pins as input with pull-up enabled. This will ensure a slow build-up of the charge in the capacitor. 2. Wait until the capacitors are almost fully charged. The exact time to wait can be calculated in advance. In addition, the pin value can be continually read until it reads a 1. This provides the earliest time possible to move to the next step. 3. Reconfigure the pins as output. When changing the direction, the value that is output on the pin is not taken from the corresponding register. Instead, it is sampled from what was provided when the pin was still an input. If the capacitor is not sufficiently charged, it will output a 0. If enough time was spent waiting in the second step above, the value will become a 1. The reconfiguration is necessary to provide a low resistance path between the capacitor and the internal voltage rail. This ensures the charge can be used to overcome the current peak that occurs while flashing. Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 36)

while the at least one processor and the at least one	NXP NHS31XX user manual and company-prepared collateral indicates that while the at least one processor (i.e., ARM M0+ core) and the at least one non-volatile memory (i.e., non-volatile memory) are activated (i.e., Active mode), receiving a temperature signal (i.e., readings from an integrated temperature sensor) at the at

non-volatile memory are activated: receiving a temperature signal at the at least one processor from a temperature sensor;	least one processor (i.e., ARM M0+ core) from a temperature sensor (i.e., integrated temperature sensor). **5.3.1 Active mode** Active mode is the only mode in which the ARM core is executing instructions. The system clock, or a dedicated peripheral clock, clocks the peripherals. The chip is in Active mode after reset. The reset values of the PDRUNCFG and SYSAHBCLKCTRL registers determine the default power configuration (see Section 4.5.6). The power configuration can be changed during runtime. Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 32) **7.1 About this chapter** This chapter describes the use of the temperature sensing feature of the NHS31xx family of sensor node ICs. **7.2 Introduction** The temperature sensor is integrated into the chip and can accurately measure temperatures over a wide range. **7.3 Features** The temperature sensor block measures the temperature of the die and outputs a calibrated value in Kelvin. It has a ±0.3 °C absolute temperature accuracy between 0 °C and 40 °C, and ±0.5 °C between −40 °C to +85 °C. **7.4 General description** Register base address of the temperature sensor block: 0x4006 0000. The temperature is measured using a high-precision zoom-ADC. Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 53) **7.6.1 Temperature sensor control register (CR)** **Table 60. CR register (address 0x4006 0000) bit description** | Bit | Symbol | Description | Reset value | Access | |---|---|---|---|---| | 0 | START | sensor start bit. The temperature sensor clears this bit at the end of the measurement | 0 | R/W | | 31:1 | - | (reserved) | - | - | **7.6.2 Temperature sensor data register (DR)** The DR register holds the current temperature data in either raw or calibrated format. Reading the DR register clears the temperature sensor interrupts. **Table 61. DR register (address 0x4006 0004) bit description** | Bit | Symbol | Description | Reset value | Access | |---|---|---|---|---| | 15:0 | TDATA | result of last conversion. Format depending on the TOUTMODE bit of the SP0 register. Raw format is unsigned fixed point (5.11); calibrated format is signed fixed point (10.6) 2-complement | 0x0000 | R | | 31:16 | - | (reserved) | - | - | Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 54)

could cause a malfunction resulting from exposure to higher temperatures.

An NFC tag, integrated in the NHS3100, allows the integrity of the parcel to be checked and the resulting data to be logged. Before using the drug, a pharmacist or patient can use a standalone NFC reader or an NFC-enabled smartphone, loaded with a smartphone app provided by the drug manufacturer, to check the drug's status.

Because the NHS3100 is equipped with an accurate real-time clock (RTC), the TTI system can achieve a date/time accuracy of 0.1% over the period of one year.

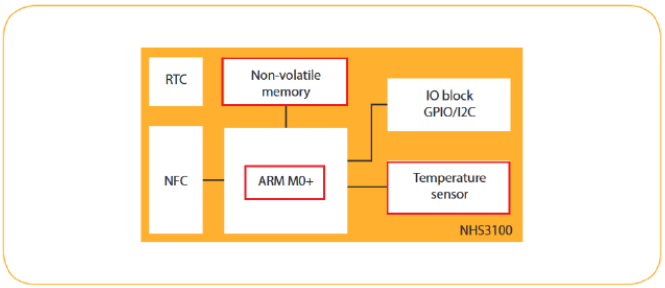
To improve the TTI's shelf life, the NHS3100 is started with an NFC command that turns on the battery. Other information can be programmed into the NHS3100 in parallel, including

The NHS3100 can be used as a passive NFC tag to provide readings from the integrated temperature sensor. This passive mode also allows the logged temperature readings to be read on the NFC reader device or smartphone without involving the TTI's battery. This helps extend the TTI's shelf life even further.

DEVELOPMENT PLATFORM

To help developers save time and effort, the NHS3100 is available in a complete design platform that includes the necessary coin battery and NFC antenna.

The NHS3100 is equipped with an ARM-based Cortex-M0+ microcontroller. The MCU is supported by the Code Red Integrated Development Environment (IDE), and is compatible with the software ecosystem associated with all industry-standard ARM cores.



NHS3100 block diagram

Source: https://www.nxp.com/docs/en/brochure/75017603.pdf

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NHS3152 power only from NFC field and load Capacitor

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tom_sander
Contributor II

Hello,

I would like to power the NHS3152 chip only through the NFC field and perform a measurement with it. Unfortunately the measurement seems to consume too much current, so I inserted a capacitor (100µF) between PIO0_7 (high-drive-pin) and ground. Now I want to charge this capacitor through the field first and then use the stored energy of the capacitor plus that of the field to perform a measurement. I have created the following program for this purpose:

Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true

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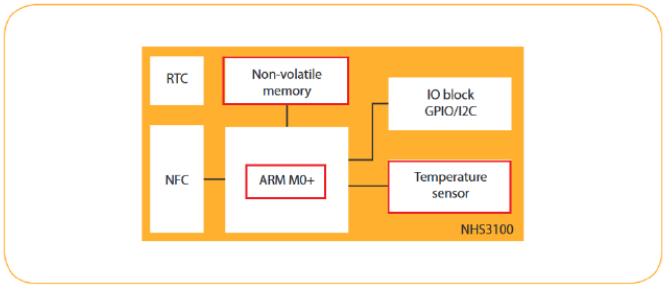
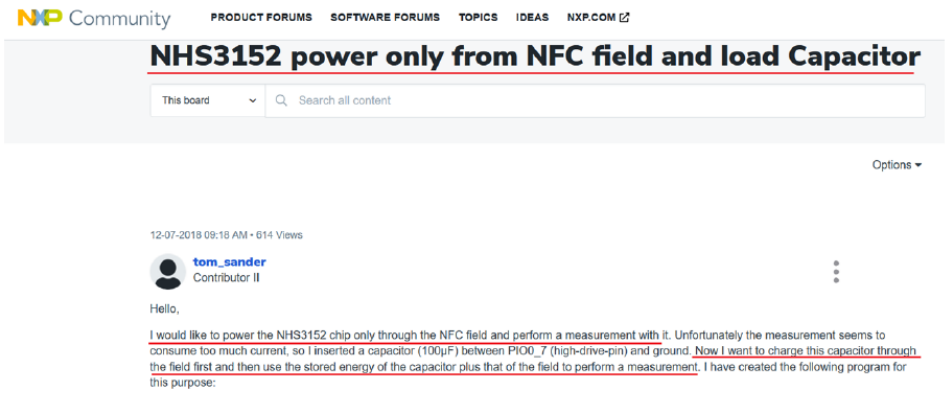
So the order would be, on the <n>-th tap:

- power-up due to NFC
- start charging of the cap
- create an NDEF message with the result of the measurements performed at tap <n-1>
- wait until the cap is charged
- start measurements
- store the result in EEPROM
- wait until the NFC field is removed and the chip dies.

Kind regards,
Dries.

Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true

storing data representative of the temperature signal in the at least one non-volatile memory; and	As per NXP NHS31xx user manual, company-prepared collateral and company reprensentative statements in NXP's community forum, it is configured to perform a method comprising, storing data (i.e., logged temperature readings) representative of the temperature signal (i.e., readings from integrated temperature sensor) in the at least one non-volatile memory (i.e., non-volatile memory, EEPROM). The logged temperature readings from the integrated temperature sensor can be read via the NFC without needing the battery from the non-volatile memory (EEPROM). could cause a malfunction resulting from exposure to higher temperatures. An NFC tag, integrated in the NHS3100, allows the integrity of the parcel to be checked and the resulting data to be logged. Before using the drug, a pharmacist or patient can use a standalone NFC reader or an NFC-enabled smartphone, loaded with a smartphone app provided by the drug manufacturer, to check the drug's status. Because the NHS3100 is equipped with an accurate real-time clock (RTC), the TTI system can achieve a date/time accuracy of 0.1% over the period of one year. To improve the TTI's shelf life, the NHS3100 is started with an NFC command that turns on the battery. Other information can be programmed into the NHS3100 in parallel, including The NHS3100 can be used as a passive NFC tag to provide readings from the integrated temperature sensor. This passive mode also allows the logged temperature readings to be read on the NFC reader device or smartphone without involving the TTI's battery. This helps extend the TTI's shelf life even further. DEVELOPMENT PLATFORM To help developers save time and effort, the NHS3100 is available in a complete design platform that includes the necessary coin battery and NFC antenna. The NHS3100 is equipped with an ARM-based Cortex-M0+ microcontroller. The MCU is supported by the Code Red Integrated Development Environment (IDE), and is compatible with the software ecosystem associated with all industry-standard ARM cores.  NHS3100 block diagram Source: https://www.nxp.com/docs/en/brochure/75017603.pdf  Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true

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So the order would be, on the <n>-th tap:

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- start charging of the cap
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- wait until the cap is charged
- start measurements
- store the result in EEPROM
- wait until the NFC field is removed and the chip dies.

Kind regards,
Dries.

Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true

Optimized for event logging	Multiple event detection mechanisms (resistive capacitive or GPIO) Event control (pin-change or wake-up)
Flexible	Customer-programmable ARM Cortex M0+ processor industry class ARM development tools
Low power	Battery start enabling via NFC (extends shelf life) Over-the-air powered (NFC)
Highly integrated	Embedded non-volatile data logging storage (up to 32KB) No crystal
Interfaces	NFC for readout and parameter writing and power GPIO pins for visual feedback (e.g. LED) SPI and I²C

Source: https://www.nxp.com/docs/en/brochure/75017700.pdf (Page: 3)

1.3 Device-dependent features

The following features are available, depending on the chip variant:

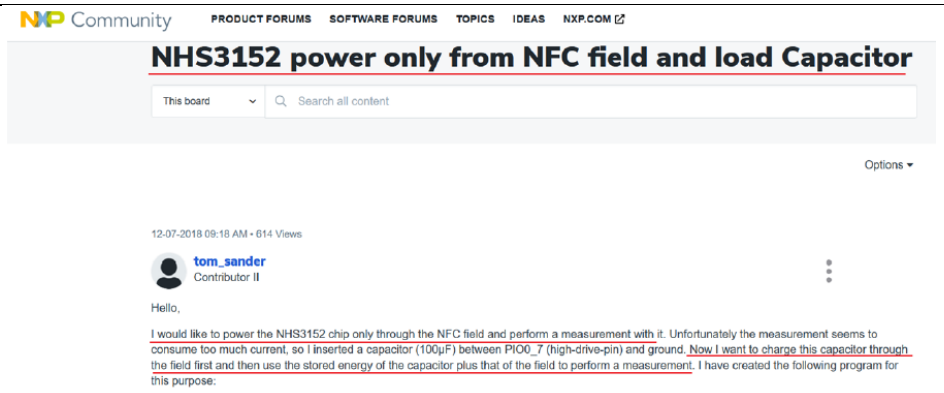
Table 2. Feature overview

Variant	Function	ADC / DAC	RTC	NFC	Temp.	I2D	SPI
NHS3100	temperature Logger	-	yes	yes	yes	-	yes
NHS3152	therapy adherence monitor - resistive	yes	yes	yes	yes	yes	yes

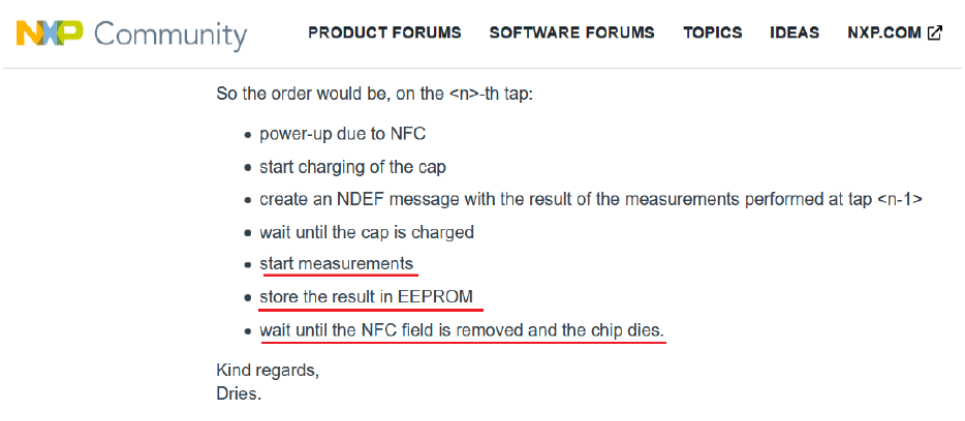
Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 5)

	7.1 About this chapter This chapter describes the use of the temperature sensing feature of the NHS31xx family of sensor node ICs. **7.2 Introduction** The temperature sensor is integrated into the chip and can accurately measure temperatures over a wide range. **7.3 Features** The temperature sensor block measures the temperature of the die and outputs a calibrated value in Kelvin. It has a ±0.3 °C absolute temperature accuracy between 0 °C and 40 °C, and ±0.5 °C between −40 °C to +85 °C. **7.4 General description** Register base address of the temperature sensor block: 0x4006 0000. The temperature is measured using a high-precision zoom-ADC. Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 53)

discharging the stored energy such that the voltage of the stored energy drops below the pre-defined threshold and turning OFF the at least one processor and the at least one non-volatile memory after the data representative of the temperature signal has been stored in the at least one non-volatile memory.	The NXP NHS31xx user manual and company representative statements in the NXP's community forum indicate the NHX31xx is configured to perform a method comprising, discharging the stored energy (i.e., utilizing the power stored in the capacitors to support operations like temperature measurement and storage) such that the voltage of the stored energy drops below the pre-defined threshold (i.e., 1.72V) and turning OFF (i.e., battery-off mode, when NFC power drops below 1.72V, chip dies) the at least one processor (i.e., ARM M0+ core) and the at least one non-volatile memory (i.e., non-volatile memory like EEPROM) after the data representative of the temperature signal has been stored (i.e., logged temperature readings) in the at least one non-volatile memory (i.e., non-volatile memory). When the NFC power is above 1.72V the device is turned on and operations like temperature measurement and storage take place. It is supported by the use of capacitors which store and energy and provide the required current whenever needed. However, once the available power is decreased below 1.72V and the capacitors are discharged, there is no other power source available to energize the processor and memory and hence, they must turn off.



Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true



Source: https://community.nxp.com/t5/NFC/NHS3152-power-only-from-NFC-field-and-load-Capacitor/m-p/846498/highlight/true

5.2 General description

The PMU controls four power modes:

- Active
- Sleep
- Deep-sleep
- Deep power-down

Additionally, the chip can be put into the Battery-off mode, which reduces current to nA levels. However, this mode can only be left via the RESETN pin or an NFC signal.

The IC power controller controls power flow from the NFC domain or the external domain to the internal domains; the PMU controls the power regulators.

Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 32)

- Power control:
  - Supply voltage range: 1.72 V to 3.6 V
  - Passive powering via NFC field possible
  - Integrated Power Management Unit (PMU) for fine-grained control of power consumption
  - Four reduced power modes: Sleep, Deep-sleep, Deep power-down and Battery-off
  - Power gating for each analog peripheral for ultra-low-power operation
  - < 50 nA current consumption with battery power switch open
  - Power-On Reset (POR)

Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 4)

18:17	FORCEVBAT FORCEVNFC	-	force the power source selection	0
		01	force to VBAT/external power	
		10	force to NFC power	
		11	autoswitching if PMULPM is 0	

Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 41)

5.4 System power architecture

The NHS31xx platform accepts power from two different sources: from the external power supply pin VDDBAT (domain VBAT), or from the built-in NFC/RFID rectifier (domain VNFC).

VDD_ALON via the VDD_ALON pad powers the external ring (VDDE) of the IO pads, as shown in Figure 8.

Note: *the pad ring does not power the VDDBAT pin, it is thus not possible to power external devices connected to this pin. In Passive RF mode, external devices can be powered by connecting them to a PIO0_n (preferably a high-drive pin) set to output logic 1.*

The PMU in the always-on domain then decides on the powering of the internal domains.

The power source decision is as follows:

- If voltage is detected on VBAT and not on VNFC, VBAT powers the internal domains
- If voltage < 1.72 V is detected on VBAT, and higher voltage is detected on VNFC, VNFC powers the internal domains
- If voltage > 1.72 V is detected at both VBAT and VNFC, VBAT powers the internal domains

Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 35)

The power-up sequence is shown in Figure 11. When external power is applied and the PSUBAT switch closed, the always-on part gets a power-on reset signal and the timer FRO starts running. The TFRO starts a small state machine in the PMU. In the first state, the LDO powering the digital domain is started. In the second state, the LDO powering the 1.6 V analog domain is started. In the last state, the system is considered 'on'. The transition from 'off' to 'on' takes approximately 92 µs. In the VDD1V2 domain, enabling the LDO1 and SFRO triggers the system_por. The system can boot when the Flash memory is operational.

If there is no external power, but there is RF power, the same procedure is followed except that PSWNFC connects power to the LDOs.

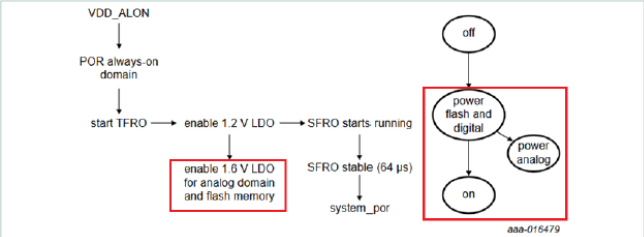


Figure 11. NHS31xx power-up sequence

Source: https://www.nxp.com/docs/en/user-guide/UM10876.pdf (Page: 39)

The VNFC input power net contains a buffer capacitor to maintain system integrity during Miller pauses when powered from RF field. Each pause lasts 3 µs, and the voltage drop should be limited to 0.4 V (1.4 V at input of 1.2 V LDO). The average current is assumed at 150 µA. In this case, the minimum size for the buffer capacitor is:

$$C = \frac{\Delta Q}{\Delta V} = \frac{150\ \mu A \times 3\ \mu s}{0.4\ V} = 1.125\ nF \qquad (1)$$

For passive RFID powered operation, adding an external 100 nF capacitor on PIO0_x pins set to logic 1 is recommended. Adding this capacitor ensures that all operations are possible during Miller pauses (e.g. Flash write).

Source: http://www.farnell.com/datasheets/2337743.pdf (Page: 36)

- The user can force the selection of the VBAT input by disabling the automatic power switch, which disables the automatic source selector voltage comparator.

When on NFC power only (passive operation), connect one or more 100 nF external capacitors in parallel to a GPIO pad and set that pad as an output driven to logic 1. A high-drive pin should preferably be chosen and several pins can be connected in parallel.

PSWNFC and PSWBAT are the power switches. PSWNFC connects power to the VDD_ALON power net when an RF field is present. PSWBAT connects power from the

Source: https://www.nxp.com/docs/en/data-sheet/NHS3100.pdf (Page: 36)

could cause a malfunction resulting from exposure to higher temperatures.

An NFC tag, integrated in the NHS3100, allows the integrity of the parcel to be checked and the resulting data to be logged. Before using the drug, a pharmacist or patient can use a standalone NFC reader or an NFC-enabled smartphone, loaded with a smartphone app provided by the drug manufacturer, to check the drug's status.

Because the NHS3100 is equipped with an accurate real-time clock (RTC), the TTI system can achieve a date/time accuracy of 0.1% over the period of one year.

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The NHS3100 can be used as a passive NFC tag to provide readings from the integrated temperature sensor. This passive mode also allows the logged temperature readings to be read on the NFC reader device or smartphone without involving the TTI's battery. This helps extend the TTI's shelf life even further.

DEVELOPMENT PLATFORM

To help developers save time and effort, the NHS3100 is available in a complete design platform that includes the necessary coin battery and NFC antenna.

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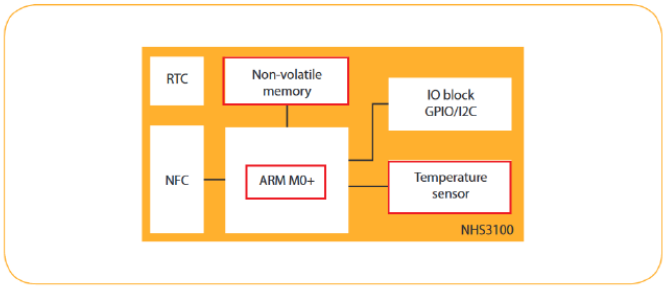

NHS3100 block diagram

Source: https://www.nxp.com/docs/en/brochure/75017603.pdf

These allegations of infringement are preliminary and are therefore subject to change.

10. NXP has and continues to induce infringement. NXP has actively encouraged or instructed others (e.g., its customers and/or the customers of its related companies), and continues to do so, on how to use its products and services (e.g., wireless temperature sensors) such as to cause

infringement of one or more of claims 1–27 of the '910 patent, literally or under the doctrine of equivalents. Moreover, NXP has known or should have known of the '910 patent and the technology underlying it from at least the date of the filing of the lawsuit.

11. NXP has and continues to contributorily infringe. NXP has actively encouraged or instructed others (e.g., its customers and/or the customers of its related companies), and continues to do so, on how to use its products and services (e.g., wireless temperature sensors) and related services such as to cause infringement of one or more of claims 1–27 of the '910 patent, literally or under the doctrine of equivalents. Moreover, NXP has known or should have known of the '910 patent and the technology underlying it from at least the date of the filing of the lawsuit.

12. NXP has caused and will continue to cause Geotag damage by direct and indirect infringement of (including inducing infringement of) the claims of the '910 patent.

IV. JURY DEMAND

Geotag hereby requests a trial by jury on issues so triable by right.

V. PRAYER FOR RELIEF

WHEREFORE, Geotag prays for relief as follows:

a. enter judgment that Defendant has infringed the claims of the '910 patent through NXP payment links;

b. award Geotag damages in an amount sufficient to compensate it for Defendant's infringement of the '910 patent in an amount no less than a reasonable royalty or lost profits, together with pre-judgment and post-judgment interest and costs under 35 U.S.C. § 284;

c. award Geotag an accounting for acts of infringement not presented at trial and an award by the Court of additional damage for any such acts of infringement;

d. declare this case to be "exceptional" under 35 U.S.C. § 285 and award Geotag its attorneys' fees, expenses, and costs incurred in this action;

e. declare Defendant's infringement to be willful and treble the damages, including attorneys' fees, expenses, and costs incurred in this action and an increase in the damage award pursuant to 35 U.S.C. § 284;

f. a decree addressing future infringement that either (i) awards a permanent injunction enjoining Defendant and its agents, servants, employees, affiliates, divisions, and subsidiaries, and those in association with Defendant from infringing the claims of the Patents-in-Suit, or (ii) awards damages for future infringement in lieu of an injunction in an amount consistent with the fact that for future infringement the Defendant will be an adjudicated infringer of a valid patent, and trebles that amount in view of the fact that the future infringement will be willful as a matter of law; and

g. award Geotag such other and further relief as this Court deems just and proper.

Respectfully submitted,

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Attorneys for Geotag IP, LLC